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doesn t map the rtl async neg reset with its counterpart in netlist dc web in this user all github daviscao conformal lec this commit does not belong to any branch on this repository and may belong to a fork outside of the repository master switch branches tags branches tags could not load branches nothing to show refname default view all branches web 4 oct 2021 there are numerous tools available in the industry to check logical equivalence but the most widely used ones are conformal from cadence and formality from synopsys apart from lec these web cadence conformal suite of tools contains a tool called logic equivalence checker or lec section 4 of this tutorial describes how to formally verify that the synthesized design is functionally equivalent to the rtl description using lec this section can be skipped if one chooses to use formality for equivalence checking during the web 1 in the setup mode load the golden and revised designs 2 change system mode to lec 3 add all ports as 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